REMARKS

1. It appears that the Examiner misunderstands the nature and function of HEYNE's circuit. At paragraph 34 of the office action, the Examiner incorrectly states that the period Tp of the input signal (IN) to HEYNE's circuit of FIG. 1 "is adjusted by the number of N or M delay elements [I1 or I2] to result in a resolution of Tp/N [t1] or Tp/M [t2]". It is not the function of HEYNE's circuit to adjust the period of its input signal. The function of HEYNE's circuit is to delay in the IN signal thereby to produce an output signal OUT. The number of delay elements in HEYNE's circuit has no effect on the period of its input signal IN; nothing in HEYNE's circuit has any influence at all on the period of the IN signal. When IN is periodic, the periods of the IN and OUT signals are the same, and HEYNE's circuit has no effect on the periods of either of those signals. Nothing anywhere in HEYNE suggests that HEYNE's circuit has any effect on any characteristic of the IN signal.

Also the number of delay elements I1 and I2 has no effect on the resolution with which HEYNE's circuit can adjust time delays. HEYNE's circuit delays the IN signal by a selected amount of time by passing it through a selected number of inverters I1 and I2 to produce output signal OUT. The total delay is equal to the sum of delays of the individual delays of the inverters I1 and I2 that the IN signal passes through. The numbers of inverters I1 and I 2 the IN signal passes through on its way to becoming the OUT signal are selected by multiplexers MUX1 and MUX2. As discussed below, the resolution with which HEYNE's circuit can adjust the delay it provides is equal to the delay of one of inverters I1 and has nothing to do with the number of inverters I1 and I2 in HEYNE's circuit.

2. At paragraph 36 (first occurrence) of the office action, the Examiner correctly points to HEYNE, col. 4, lines 39-44 as teaching "that the phase of the output OUT signal is adjusted to the phase of the input clock CLK at the input IN". But in paragraphs 36 (second occurrence) through 39 and elsewhere in the office action, the Examiner incorrectly concludes that the fact that HEYNE's circuit brings the OUT signal into phase with the IN signal would somehow lead one of skill in the art to conclude that the delays of inverters I1 and I2 must be "integer fractions of the period of [the IN] signal in

order to have a practical apparatus that can incrementally adjust the delay circuit to achieve synchronization". The Examiner's conclusion is incorrect for the following three reasons.

a. The first reason is that based on HEYNE's schematic, one of skill in the art would see that the IN signal period has no effect on the delays provided by inverters I1 and I2. Note, in contrast, that in the applicant's circuit of FIGs. 5, 7 and 8, the period of the input signal (ROSC) very clearly does influence the delays provided by gates 60 and 68. Phase lock loop circuits set them to Tp/N and Tp/M, where Tp is the period of the ROSC signal, and M and N are integers. But in HEYNE's circuit there is no disclosed mechanism for controlling the delays of inverters I1 and I2 so that they are integer fractions of the period of the IN signal. Thus one of skill in the art looking at HEYNE's circuit schematic would not conclude that the delays of inverters I1 and I2 have any particular relationship to the period of the IN signal.

b. The second reason why one of skill in the art would not conclude that inverters I1 and I2 have periods Tp/N and Tp/M, even though HEYNE says that the delay circuit is adjusted to bring OUT into phase with IN, has to do with what persons of skill in the electronic arts understand with respect to resolution when speaking of signal characteristics. To explain, let us first consider a simple analogy. If we measure the voltage of a signal with a digital voltmeter having a resolution of 0.1 volt and the voltmeter gives a reading of 5.0 volts, then one of skill in the art would say that "the signal has a voltage of 5.0 volts", but one of skill in the art would understand that the true signal voltage could be anywhere from 4.95 to 5.05 volts. In other words, when those of skill in the art say a signal is 5.0 volts, there is an implicit understanding that the signal is approximately 5.0 volts within the resolution of the device used to measure it or within the resolution with which the device that controls signal voltage can adjust that voltage. In general, those of skill in the electronic arts understand that whenever we say that some parameter of a signal has a particular magnitude, that the magnitude is only approximate and lies within some range determined by the resolution with which that magnitude is measured or selected. Thus when HEYNE says that the number of inverters I1 and I2 in the signal path of the IN signal can be selected to bring the OUT signal into

phase with the IN signal, one of ordinary skill in the electronic arts would understand that OUT and IN would have the "same" phase only to the extent that the HEYNE's circuit is able to resolve its delay adjustment. The Examiner correctly points out that HEYNE's circuit can only make delay adjustments incrementally, and one of skill in the art would understand that the smallest amount by which HEYNE's circuit can increase or decrease its signal delay is clearly the unit delay of one inverter I1 or I2, whatever that unit delay may be. But HEYNE provides no reason for one skilled in the art to conclude that the inverter delay is an integer fraction of the period of the IN signal, or indeed that it would have any particular relationship to the period of the IN signal.

c. The third, and perhaps most important, reason the Examiner's assertion that HEYNE's statement about bringing OUT into phase with IN teaches one of skill in the art that the inverter delays are Tp/M and Tp/N is incorrect is because HEYNE directly teaches us that the inverter delays are chosen on another basis. The Examiner, at paragraph 37 requests the applicant to "verify that HEYNE did not disclose such contrary notions anywhere in the disclosure". The applicant is unable to satisfy the Examiner's request because the "contrary notion" is in fact very clearly disclosed at HEYNE column 5, line 49 - col. 6, line 2. This section of HEYNE teaches the following:

a. The delay of HEYNE's delay circuit varies due to temperature fluctuations,

b. The delay t2 of each inverter I2 should equal to the maximum fluctuation range of the delay time of the entire delay unit T due to temperature fluctuations, and

c. The sum of delays t1 of inverters I1 should be at least equal t2.

Thus one of skill in the art would conclude that delays t1 and t2 of inverters I1 and I2 vary with temperature and have no relationship to the period or any other parameter of the IN signal. HEYNE instead indicates that the delays of inverters t1 and t2 should be chosen as functions of the maximum temperature dependant fluctuation range of the entire delay circuit, and teaches away from the notion that the

delays of inverters t1 and t2 are or should be set to integer fractions of the period of the IN signal.

3. At paragraph 39 of the office action, the Examiner continues to maintain that FIG. 3 of HEYNE teaches that for HEYNE's circuit M and N are the relatively prime integers 5 and 12. The Examiner correctly observes that 5 and 12 are relatively prime, however the Examiner does not clearly explain how HEYNE FIG. 3 or any other part of HEYNE teaches that inverters I1 and I2 have delays Tp/M and Tp/N where M = 5 and N = 12. As discussed below, FIG. 3 and other parts of HEYNE clearly show that M and N are not relatively prime and therefore could not possibly be 5 and 12.

Consistent with the terminology employed in the applicant's specification and claims, let us first assume HEYNE's input signal IN is periodic and has a period of Tp, let us define M in HEYNE's circuit as the ratio of Tp to the unit delay t1 of each of inverters I1, and let us define N as the ratio of the period of the IN signal to the unit delay t2 of each of inverter I2. If we want to compute M and N for HEYNE's circuit from HEYNE's FIG. 3, FIG. 3 must tell us something about the magnitudes of t1 and, t2 relative to the period of the IN signal. But while FIG. 3 graphically depicts magnitudes of t1 and t2 relative to one another, it does not depict the magnitude of the IN signal period relative to t1 and t2. No graphical representation of the IN signal period appears in FIG. 3. Thus it is not possible to determine any particular values for M and N from the information contained in FIG. 3 because it is not possible to determine from FIG. 3 (or from any part of HEYNE) a ratio of either t1 or t2 to the period Tp of the IN signal. The Examiner's position that HEYNE's FIG. 3 teaches M and N of 5 and 12 is therefore clearly incorrect.

Moreover, while we cannot determine the values of M and N from HEYNE's FIG. 3, or even whether they are integers, we can nonetheless determine from FIG. 3 that for HEYNE's circuit, M and N are definitely not relatively prime. FIG. 3 teaches that the ratio t1/t2 is ¼, since the right hand side of FIG. 3 shows four t1 intervals are equal in length to a single t2 interval. This implies that

$$t1/t2 = (Tp/M)/(Tp/N) = (N/M) = \tfrac{1}{4} .$$

This proves that for HEYNE M and N, whatever they may be, are not relatively prime since M must be an integer multiple (4) of N in order for N/M to be ¼ and because by definition, two numbers cannot be relatively prime if one is an integer multiple of the other. Thus HEYNE's FIG. 3 clearly teaches that M and N are <u>not</u> relatively prime. HEYNE's discussion at col. 5, line 49 - col. 6, line 2 also teaches exactly the same thing, that t1/t2 = ¼, which also implies that M and N for HEYNE's circuit are not relatively prime.

4. The Examiner continues to maintain in paragraph 41 that HEYNE's abstract indicates that the delay ranges provided by inverters I1 and I 2 are the functions of Tp, N and M as recited in claim 4. In particular, the Examiner's paragraph 41 asserts certain mathematical terms (Tp, 5/3Tp, 5*4t1, 12t1) in some way describe the delay ranges of HEYNE's circuit provided by inverters I1 and I2, even though no such mathematical terms appear in HEYNE's abstract, in HEYNE's FIG. 3 or anywhere else in HEYNE, even though no such terms can be derived from any information provided by HEYNE, and even though such mathematical terms appear to be expressions of discrete values rather than ranges. What in HEYNE suggests a delay "range" of Tp? What in HEYNE suggests a delay "range" of 5/3Tp? What in HEYNE suggests a delay "range" of 5*4t1? What in HEYNE suggests a delay range of "12t1"? The Examiner does not explain any of these expressions or how he arrived at them based on what appears in HEYNE's abstract, FIG. 3 or any other part of HEYNE.

HEYNE is in fact quite explicit about the delay ranges his circuit provides at col. 5, line 50 through col. 6, line 2. HEYNE tells us that the unit delay t2 of each inverter I2 is equal to the maximum fluctuation range of the delay time of the entire delay circuit resulting from temperature influences (let's call it Dtemp). Thus the range of adjustment provided by the set of inverters t2 is clearly K * Dtemp, where K is the number of inverters I2. HEYNE also says the sum of delay t1 of each inverters I1 is equal to t2. Thus inverters I1 collectively provide a delay range of t2 = Dtemp. Therefore the two delay ranges provided by inverters I2 and I1 of HEYNE's circuit are K*Dtemp and Dtemp. Since neither K nor Dtemp have any relationship with Tp, M or N, it cannot be said that HEYNE teaches the delay ranges recited in claim 4 which are functions of Tp,

M and N, and which have nothing to do with the temperature variations upon which HEYNE's delay ranges are based.

5. Claims 1-8, 11, 15-16, 20-27, 30 and 34-35 are rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 6,194,928 (HEYNE), in view of U.S. Patent 4,255,790 (HONDEGHEM). The Examiner is respectfully requested to withdraw the rejection of these claims in view of the following comments.

Claims 1, 3, 4, 6, 15, 20, 22, 23, 25, 30 and 34

The Examiner incorrectly asserts that HEYNE (FIG. 3 and col. 4, lines 39-44) teaches a first means capable of adjustably delaying a pulse with a resolution of Tp/N and a second means capable of adjustably delaying a pulse with a resolution of Tp/M where M and N are differing integers greater than 1 and Tp is the period of a pulse sequence being delayed The applicant's discussion in sections 1 and 2 above explain why the Examiner's assertion is incorrect.

The Examiner correctly concedes that HEYNE does not disclose that the programmable sequencer varies the magnitude of the first and second control data sequences in a repetitive manner as recited in claims 1, 1, 3, 4, 6, 15, 20, 22, 23, 25, 30 and 34.

The Examiner incorrectly points to HONDEGHEM (FIGs. 2 and 3; col. 4, line 62 - col. 5, line 57; and col. 5, lines 20-57) as teaching that CPU 70, RAM 84, I/O logic 112 and other associated circuits are "for changing a magnitude of the first control data [116] and a magnitude of the second control data [118] in response to each pulse of the first pulse sequence [76] such that the magnitudes of the first and second control data vary repetitively in a programmably adjustable manner" as recited in the applicant's claims 1, 15, 20, and 34. FIG. 2 shows that control data lines 116 and 118 connecting I/O logic 112 to period clock selector 108, and "sub interval clock selector" 110 but FIG. 2 provides no indication as to the function or behavior of any control data that may be carried on lines 116 and 118. FIG. 3 provides no teaching regarding control data lines 116 and 118. Col. 4, line 62 - col. 5, line 57 mention control data lines 116 and 118 only at col. 5, lines 34-36 but teach only that control lines connect I/O logic circuits 112 to devices 108 and 110 and provide no

indication as to the function of control data lines 116 and 118. The cited col. 6, lines 20-57 makes no mention whatsoever of control data lines 116 and 118. HONDEGHEM says that I/O logic 112 supplies signals from CPU 70 to unspecified circuit elements on timer board 58 (col. 5, lines 31-35), but what sort of signals appear on lines 116 and 118, and for what purpose? The Examiner asserts that control data lines 116 and 118 convey control data "that varies in a programmably adjustable manner". But other than indicating that control data lines 116 and 118 connect I/O logic 112 to devices 108 and 110 at col. 4, lines 34-36 and in FIG. 2, HONDEGHEM provides no indication as to the function of control data lines 116 and 118, or to the nature, behavior or the purpose of such control data, if any, conveyed on those control lines as input to devices 108 and 110. Moreover, there is no clear indication anywhere in HONDEGHEM as to the function of the devices 108 and 110 to which the control lines 116 and 118 are connected. Are devices 108 and 110 even remotely similar in function to any element of the applicant's claims? Who can say? HONDEGHEM does not explain what devices 108 and 110 do. Note, for example, that FIG. 2 shows devices 108 and 110 have inputs but no outputs. How would the fact that CPU 70 might use some unspecified control data to control devices 108 and 110 that perform some unspecified function motivate one of skill in the art to modify HEYNE to vary the control data input to the Mux1 and Mux2 in the manner recited in the applicant's claims?

The Examiner incorrectly maintains that the reference to "X10" in HONDEGHEM's FIG. 2 and in col. 6 lines 26-27 implies that control data lines 116 and 118 convey repetitive control data as recited in the applicant's claims. HONDEGHEM states in the cited lines only that "X10 appearing as a subscript for the first sequence is to be repeated ten times." Of course this means that the "first sequence" is repetitive, but what is this "first sequence" of which HONDEGHEM speaks? Is this a control data sequence appearing on either of control data lines 116 and 118, as the Examiner seems to suggest? No. The "first sequence" is a sequence of pulses A1 - E1 as shown in FIG. 3 that are supplied as input to a D/A converter 162 of FIG. 2 (col. 6, lines 20-26). The applicant does not claim applying a repetitive sequence to a D/A converter. The applicant's claims have nothing to do with controlling D/A converters. Thus the cited section of HONDEGHEM says nothing about any data appearing on control lines 116

and 118. Moreover, nothing anywhere in HONDEGHEM teaches anything about supplying repetitive first and second control data sequences as input to circuits having the nature and function of the first and second control means recited in the applicant's claims.

The Examiner therefore incorrectly relies on HONDEGHEM to overcome the Examiner's admission that such teaching is lacking in HEYNE.

Claims 2, 5, 21, 24 and 34

Claims 2, 5, 21, 24 and 34 recite that M and N are relatively prime, and the Examiner rejects these claims asserting that HEYNE's FIG. 3 "clearly shows that M and N are relatively prime" for HEYNE's circuit. The applicant's discussion in section 3 above explain why the Examiner's assertion is incorrect and show that HEYNE actually teaches that M and N should not be relatively prime. Thus claims 2, 5, 21, 24 and 34 are patentable over HEYNE and HONDEGHEM because the cited references do not teach M and N are relatively prime, and because HEYNE teaches away from M and N being relatively prime.

Claims 7, 8 and 16

Claims 7, 8 and 16 recite that the gates in the first or second means have switching delays of Tp/N or Tp/M where N and M are integers. The Examiner points to HEYNE abstract and col. 3, line 50 as teaching this. However, while HEYNE's abstract describes first and second delay elements, it does not indicate that their delay times are integer fractions of the period of any particular signal. Col. 3 line 50 simply indicates that the delay elements have delay times t1 and t2, but does not teach or suggest that either delay time is an integer fraction of the period of any signal or any other value. As noted in the applicant's discussion in sections 1 and 2 above, HEYNE teaches away from setting switching delays as integer fractions of the period of the IN signal.

Claims 11, 26, 27 and 35.

Claims 11, 26, 27 and 35 depend on claims 1, 20 or 34 and are patentable over the cited references for similar reasons. Claims 11, 26, 27 and 35 further recite first gates, each having a switching delay of Tp/N and/or second gates each having a switching delay of

Tp/M. HEYNE discloses first and second gates, but as discussed in sections 1 and 2 above, HEYNE teaches away from setting switching delays as functions of the period of the IN signal.

6. Claims 9-10, 12-14, 17-19, 28-29, 31-33 and 36-38 are rejected under 35 USC 103(a) as being unpatentable over HEYNE and HONDEGHEM in view of U.S. Patent 5,741,165 (LIEDBERG). The Examiner is respectfully requested to withdraw the rejection of these claims in view of the following comments.

Claims 9-10, 12-14, 17-19, 28-29, 31-33 and 36-38.

Claims 9-10, 12-14, 17-19, 28-29, 31-33 and 36-38 depend on claim 8, and for the reasons cited above, the Examiner incorrectly relies on HEYNE and HONDEGHEM as disclosing the subject matter of base claim 8. Claims 9-10, 12-14, 17-19, 28-29, 31-33 and 36-38 further recite M third gates connected in series for delaying the first pulse sequence wherein the second and third gates have similar switching delay Tp/M set by a control signal applied as input to all second and third gates. These claims are best understood with reference to the applicant's FIG. 7. The "second gates are gates 62 and the "third gates" are gates 68. The sole purpose of gates 68 is to help controller 70 to determine the proper level for signal CONTROL (B) for controlling the delays of gates 60 so that they provide the desired delay Tp/M, where M is an integer equal to the number of gates 68 and Tp is the frequency of clock signal ROSC. LIEDBERG discloses a delay circuit at FIG. 2 (FIG. 6A provides a simpler view) including a set of gates D1, D2, D3 connected in series for delaying the input signal S0 to produce output signals S1, S2 and S3 that are evenly spaced in phase as illustrated in FIG. 6B. Control device 1 compares S3 to S0 and adjusts the delays of D1-D3 so that S3 is in phase with S0, thereby ensuring that S1-S3 are evenly spaced in phase. This circuit would be similar to the applicant's FIG. 8 if LIEDBERG's logic gate 60 of FIG. 6A were replaced with the applicant's multiplexer 110. However the applicant's claim 9 relates to the applicant's circuit of FIG. 7 rather than to the circuit of FIG. 8. The circuit of FIG. 8 incorporates elements of LIEDBERG's circuit of FIG. 6A since it includes controller 70 and gates 68 (the "third gates of claim 9) having the same functions as LIEDBERG's controller 1 and delay devices

D1-D3. But the applicant's circuit of FIG. 7 also includes another set of gates 62 (the "second gates" of claims 9 and 10) not found in LIEDBERG's circuit. Note that all gates D1-D3 in LIEDBERG's circuit delay the same signal S0 while in the applicant's circuit of FIG. 7, gates 68 delay the ROSC signal and gates 62 delay the CLOCK signal. Claims 9, 10, and 12-14 clearly recite that the second and third gates delay <u>different</u> signals, not the same signal. Hence LIEDBERG fails to teach the additional limitations of claims 9-10, 12-14, 17-19, 28-29, 31-33 and 36-38.

7. In view of the foregoing remarks, it is believed that the application is in condition for allowance. Notice of Allowance is therefore respectfully requested.

Respectfully submitted,

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